

## High Voltage Class H Ceramic Speaker Driver with Automatic Level Control

### General Description

The LM48560 is a high voltage, high efficiency, Class H driver for ceramic speakers and piezo actuators. The LM48560's Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides 30V<sub>P-P</sub> output drive while consuming just 4mA of quiescent current from a 3.6V supply.

The LM48560 features National's unique automatic level control (ALC) that provides output limiter functionality. The LM48560 features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I<sup>2</sup>C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs.

The LM48560 has a low power shutdown mode that reduces quiescent current consumption to 0.1µA. The LM48560 is available in an ultra-small 16-bump micro SMD package (1.97mm x 1.97mm).

### Key Specifications

- Output Voltage at V<sub>DD</sub> = 3.6V  
R<sub>L</sub> = 1.5µF+10Ω, THD+N ≤ 1%      30V<sub>P-P</sub> (typ)
- Quiescent Power Supply Current  
at 3.6V (ALC enabled)      4mA (typ)
- Power Dissipation at 25V<sub>P-P</sub>      1W (typ)
- Shutdown current      0.1µA (typ)

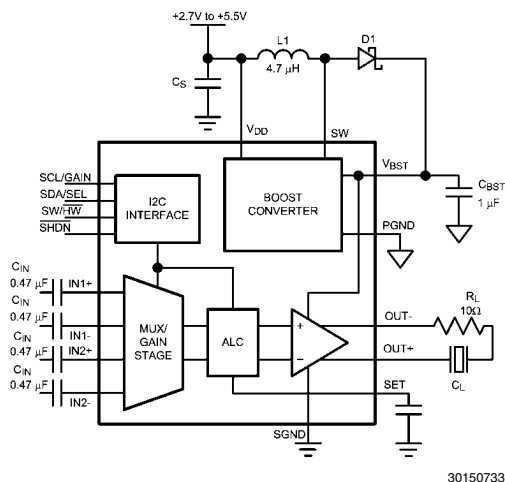
### Typical Application

### Features

- Class H Topology
- Integrated Boost Converter
- Bridge-Tied Load (BTL) Output
- Selectable Differential Inputs
- Selectable Control Interfaces (Hardware or Software mode)
- I<sup>2</sup>C Programmable ALC
- Low Supply Current
- Minimum External Components
- Micro-Power Shutdown
- Available in Space-Saving micro SMD Package

### Applications

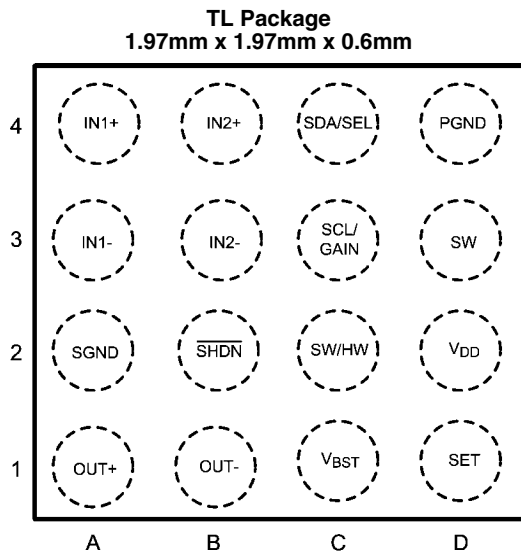
- Touch screen Smart Phones
- Tablet PCs
- Portable Electronic Devices
- MP3 Players



**FIGURE 1. Typical Application Circuit**

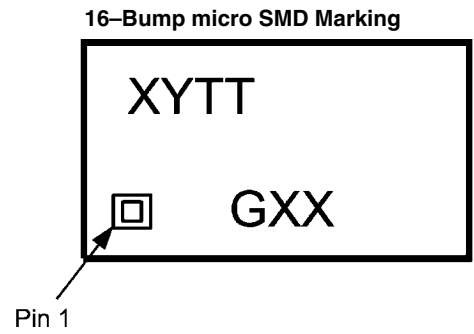
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## Connection Diagrams



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**Top View**  
 Order Number LM48560TL  
 See NS Package Number TLA16Z1A



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**Top View**  
 XY = Date code  
 TT = Die traceability  
 G = Boomer Family  
 XX = LM48560TL

## Ordering Information

**Ordering Information Table**

| Order Number | Package           | Package Drawing Number | Transport Media             | MSL Level | Green Status    |
|--------------|-------------------|------------------------|-----------------------------|-----------|-----------------|
| LM48560TL    | 16 Bump $\mu$ SMD | TLA16Z1A               | 250 units on tape and reel  | 1         | RoHS & no Sb/Br |
| LM48560TLX   | 16 Bump $\mu$ SMD | TLA16Z1A               | 2500 units on tape and reel | 1         | RoHS & no Sb/Br |

**TABLE 1. Bump Descriptions**

| Bump | Name                             | Description   |
|------|----------------------------------|---|
| A1   | OUT+                             | Amplifier Non-Inverting Output  |
| A2   | SGND                             | Amplifier Ground  |
| A3   | IN1-                             | Amplifier Inverting Input 1   |
| A4   | IN1+                             | Amplifier Non-Inverting Input 1   |
| B1   | OUT-                             | Amplifier Inverting Output  |
| B2   | $\overline{\text{SHDN}}$         | Active Low Shutdown. Connect $\overline{\text{SHDN}}$ to GND to disable device.<br>Connect $\overline{\text{SHDN}}$ to $V_{\text{DD}}$ for normal operation |
| B3   | IN2-                             | Amplifier Inverting Input 2   |
| B4   | IN2+                             | Amplifier Non-Inverting Input 2   |
| C1   | $V_{\text{BST}}$                 | Boost Converter Output  |
| C2   | $\text{SW}/\overline{\text{HW}}$ | Mode Selection Control:<br>$\text{SW}/\overline{\text{HW}} = 0 \rightarrow$ Hardware Mode<br>$\text{SW}/\overline{\text{HW}} = 1 \rightarrow$ Software Mode |
| C3   | SCL/GAIN                         | I <sup>2</sup> C Serial Clock Input (Software Mode)<br>Gain Select Input (Hardware Mode)<br>see ( <a href="#">Table 3</a> )                                 |
| C4   | SDA/SEL                          | I <sup>2</sup> C Serial Data Input (Software Mode)<br>Amplifier Input Select (Hardware Mode)<br>see ( <a href="#">Table 3</a> )                             |
| D1   | SET                              | ALC Timing Input  |
| D2   | $V_{\text{DD}}$                  | Power Supply  |
| D3   | SW                               | Boost Converter Switching Node  |
| D4   | PGND                             | Boost Converter Ground  |

## Absolute Maximum Ratings *(Note 1, Note 2)*

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

|   |                                 |
|---|---------------------------------|
| Supply Voltage <i>(Note 1)</i>                          | 6V                              |
| SW Voltage  | 25V                             |
| V <sub>BST</sub> Voltage                                | 21V                             |
| Input Voltage   | -0.3V to V <sub>DD</sub> + 0.3V |
| Power Dissipation <i>(Note 3)</i>                       | Internally limited              |
| ESD Rating, Human Body Model <i>(Note 4)</i>            | 2kV                             |
| ESD Rating, Machine Model <i>(Note 5)</i>               | 100V                            |
| ESD Rating, Charge Device Model <i>(Note 6)</i>         | 500V                            |
| Storage Temperature                                     | -65°C to + 150°C                |
| Junction Temperature                                    | 150°C                           |
| Thermal Resistance                                      |                                 |
| θ <sub>JA</sub> (TLA16Z1A)                              | 55 °C/W                         |
| Soldering Information                                   |                                 |
| See AN-1112 "Micro SMD Wafer Level Chip Scale Package." |                                 |

## Operating Ratings

|  |                                |
|--|--------------------------------|
| Temperature Range                                    |                                |
| T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub> | -40°C ≤ T <sub>A</sub> ≤ +85°C |
| Supply Voltage                                       |                                |
| V <sub>DD</sub>                                      | 2.7V ≤ V <sub>DD</sub> ≤ 5.5V  |

## Electrical Characteristics V<sub>DD</sub> = 3.6V *(Note 1, Note 2)*

The following specifications apply for R<sub>L</sub> = 1.5μF + 10Ω, C<sub>BST</sub> = 1μF, C<sub>IN</sub> = 0.47μF, C<sub>SET</sub> = 100nF, A<sub>V</sub> = 24dB unless otherwise specified. Limits apply for T<sub>A</sub> = 25°C.

| Symbol          | Parameter                          | Conditions                                       | LM48560             |                     |                     | Units (Limits) |
|-----------------|------------------------------------|--|---------------------|---------------------|---------------------|----------------|
|                 |                                    |  | Min <i>(Note 8)</i> | Typ <i>(Note 7)</i> | Max <i>(Note 8)</i> |                |
| V <sub>DD</sub> | Supply Voltage Range               |  | 2.7                 |                     | 5.5                 | V              |
| I <sub>DD</sub> | Quiescent Power Supply Current     | V <sub>IN</sub> = 0V, R <sub>L</sub> = ∞         |                     |                     |                     |                |
|                 |                                    | ALC Enabled                                      |                     | 4                   | 6                   | mA             |
|                 |                                    | ALC Disabled                                     |                     | 3.6                 |                     | mA             |
| P <sub>D</sub>  | Power Consumption                  | V <sub>OUT</sub> = 25V <sub>P-P</sub> , f = 1kHz |                     | 1                   |                     | W              |
| I <sub>SD</sub> | Shutdown Current                   | Software Mode                                    |                     | 2.5                 | 4.4                 | μA             |
|                 |                                    | Hardware Mode                                    |                     | 0.1                 | 2                   | μA             |
| T <sub>WU</sub> | Wake-up Time                       | From Shutdown                                    |                     | 15                  |                     | ms             |
| V <sub>OS</sub> | Differential Output Offset Voltage | A <sub>V</sub> = 24V                             |                     | 10                  | 90                  | mV             |
|                 |                                    | A <sub>V</sub> = 0dB (Boost Disabled)            |                     | 5                   | 20                  | mV             |

| Symbol               | Parameter                                  | Conditions  | LM48560         |                 |                 | Units<br>(Limits)      |  |
|----------------------|--|---|-----------------|-----------------|-----------------|------------------------|--|
|                      |  |   | Min<br>(Note 8) | Typ<br>(Note 7) | Max<br>(Note 8) |                        |  |
| $A_V$                | Gain (Hardware Mode)                       | IN1<br>GAIN = 0                                     | 0.5             | 0               | 0.5             | dB                     |  |
|                      |  | GAIN = 1  | 5.5             | 6               | 6.5             | dB                     |  |
|                      |  | IN2<br>GAIN = 0                                     | 23.5            | 24              | 24.5            | dB                     |  |
|                      |  | GAIN = 1  | 29.5            | 30              | 30.5            | dB                     |  |
|                      | Gain (Software Mode)                       | Boost Disabled                                      |                 |                 |                 |                        |  |
|                      |  | GAIN1 = 0, GAIN0 = 0                                | -0.5            | 0               | 0.5             | dB                     |  |
|                      |  | GAIN1 = 0, GAIN0 = 1                                | 5.5             | 6               | 6.5             | dB                     |  |
|                      |  | GAIN1 = 1, GAIN0 = 0                                | 11.5            | 12              | 12.5            | dB                     |  |
|                      |  | GAIN1 = 1, GAIN0 = 1                                | 17.5            | 18              | 18.5            | dB                     |  |
|                      |  | Boost Enabled                                       |                 |                 |                 |                        |  |
| GAIN1 = 0, GAIN0 = 0 | 20.5                                       | 21  | 21.5            | dB              |                 |                        |  |
| GAIN1 = 0, GAIN0 = 1 | 23.5                                       | 24  | 24.5            | dB              |                 |                        |  |
| GAIN1 = 1, GAIN0 = 0 | 26.5                                       | 27  | 27.5            | dB              |                 |                        |  |
| GAIN1 = 1, GAIN0 = 1 | 29.5                                       | 30  | 30.5            | dB              |                 |                        |  |
|                      | Gain Step Size<br>(Software Mode)          |   |                 | 3               |                 | dB                     |  |
| $R_{IN}$             | Input Resistance                           | $A_V = 0\text{dB}$<br>$A_V = 30\text{dB}$           | 46<br>46        | 50<br>50        | 58<br>58        | $k\Omega$<br>$k\Omega$ |  |
| $V_{OUT}$            | Output Voltage                             | THD+N = 1%  |                 |                 |                 |                        |  |
|                      |  | $f = 200\text{Hz}$<br>$f = 1\text{kHz}$             | 25              | 30<br>30        |                 | $V_{P-P}$<br>$V_{P-P}$ |  |
| THD+N                | Total Harmonic Distortion + Noise          | $V_{OUT} = 18V_{P-P}$ , $f = 1\text{kHz}$           |                 | 0.08            |                 | %                      |  |
| PSRR                 | Power Supply Rejection Ratio<br>(Figure 2) | $V_{DD} = 3.6V + 200mV_{P-P}$ sine, Inputs = AC GND |                 |                 |                 |                        |  |
|                      |  | $f_{RIPPLE} = 217\text{Hz}$                         | 55              | 78              |                 | dB                     |  |
|                      |  | $f_{RIPPLE} = 1\text{kHz}$                          |                 | 76              |                 | dB                     |  |
| CMRR                 | Common Mode Rejection Ratio<br>(Figure 3)  | $V_{CM} = 200mV_{P-P}$ sine                         |                 |                 |                 |                        |  |
|                      |  | $f_{RIPPLE} = 217\text{Hz}$                         |                 | 68              |                 | dB                     |  |
|                      |  | $f_{RIPPLE} = 1\text{kHz}$                          |                 | 78              |                 | dB                     |  |
| SNR                  | Signal-to-Noise-Ratio                      | Boost Disabled, A-weighted                          |                 | 107             |                 | dB                     |  |
|                      |  | Boost Enabled A-weighted                            |                 | 98              |                 | dB                     |  |
| $\epsilon_{OS}$      | Output Noise                               | A-weighted<br>$A_V = 24\text{dB}$                   |                 | 134             |                 | $\mu V_{RMS}$          |  |
|                      |  | $A_V = 0\text{dB}$ (Boost Disabled)                 |                 | 16              |                 | $\mu V_{RMS}$          |  |
| $T_A$                | Attack Time                                | ATK1:ATK0 = 00, $C_{SET} = 100\text{nF}$            |                 | 0.83            |                 | ms                     |  |
| $T_R$                | Release time                               | RLT1:RLT0 = 00, $C_{SET} = 100\text{nF}$            |                 | 0.5             |                 | s                      |  |
| $f_{SW}$             | Boost Converter Switching Frequency        |   |                 | 2               |                 | MHz                    |  |
| $I_{LIMIT}$          | Boost Converter Current Limit              |   |                 | 1.5             |                 | A                      |  |
| $V_{IH}$             | Logic High Input Threshold                 | SHDN  | 1.4             |                 |                 | V                      |  |
| $V_{IL}$             | Logic Low Input Threshold                  | SHDN  |                 |                 | 0.5             | V                      |  |
| $I_{IN}$             | Input Leakage Current                      | SHDN  |                 | 0.1             | 0.2             | $\mu A$                |  |

## I<sup>2</sup>C Interface Characteristics (Note 1, Note 2)

The following specifications apply for  $R_{PU} = 1k\Omega$  to  $V_{DD}$ ,  $SW/HW = 1$  (Software Mode) unless otherwise specified. Limits apply for  $T_A = 25^\circ\text{C}$ .

| Symbol   | Parameter                  | Conditions | LM48560                        |                                |                                | Units<br>(Limits) |
|----------|----------------------------|------------|--------------------------------|--------------------------------|--------------------------------|-------------------|
|          |                            |            | Min<br><small>(Note 7)</small> | Typ<br><small>(Note 6)</small> | Max<br><small>(Note 7)</small> |                   |
| $V_{IH}$ | Logic Input High Threshold | SDA, SCL   | 1.1                            |                                |                                | V                 |
| $V_{IL}$ | Logic Input Low Threshold  | SDA, SCL   |                                |                                | 0.5                            | V                 |
|          | SCL Frequency              |            |                                |                                | 400                            | kHz               |
| $t_1$    | SCL Period                 |            | 2.5                            |                                |                                | $\mu\text{s}$     |
| $t_2$    | SDA Setup Time             |            | 250                            |                                |                                | ns                |
| $t_3$    | SDA Stable Time            |            | 250                            |                                |                                | ns                |
| $t_4$    | Start Condition Time       |            | 250                            |                                |                                | ns                |
| $t_5$    | Stop Condition Time        |            | 250                            |                                |                                | ns                |

**Note 1:** “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the given in *Absolute Maximum Ratings*, whichever is lower.

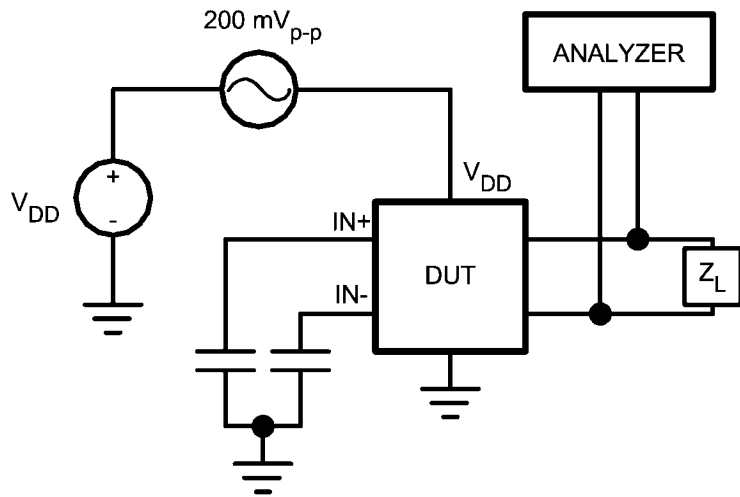
**Note 4:** Human body model, applicable std. JESD22-A114C.

**Note 5:** Machine model, applicable std. JESD22-A115-A.

**Note 6:** Charge device model, applicable std. JESD22-C101-C.

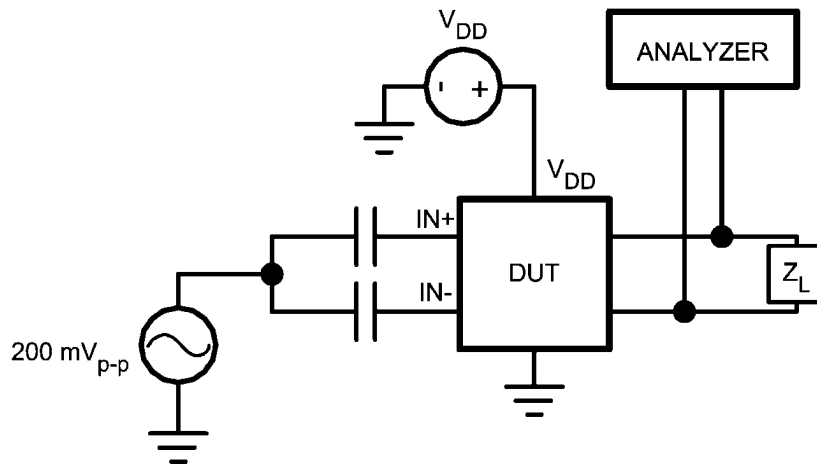
**Note 7:** Typical values represent most likely parametric norms at  $T_A = +25^\circ\text{C}$ , and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

**Note 8:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.



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FIGURE 2. PSRR Test Circuit

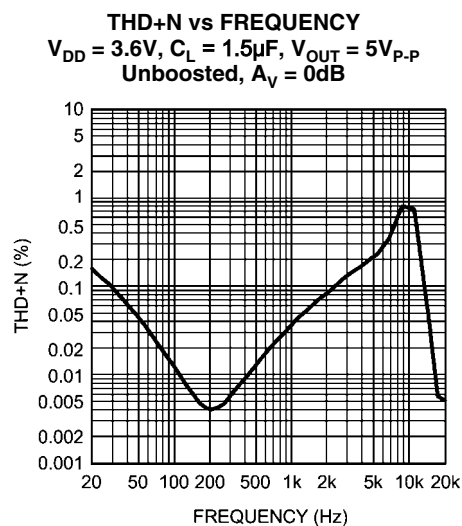
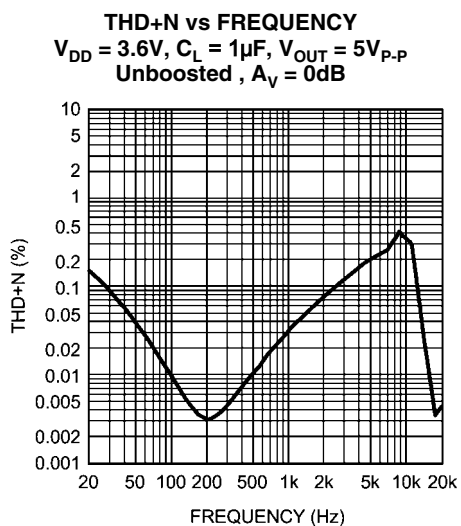
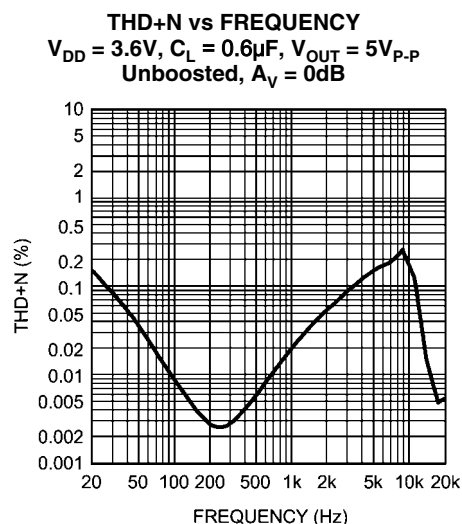
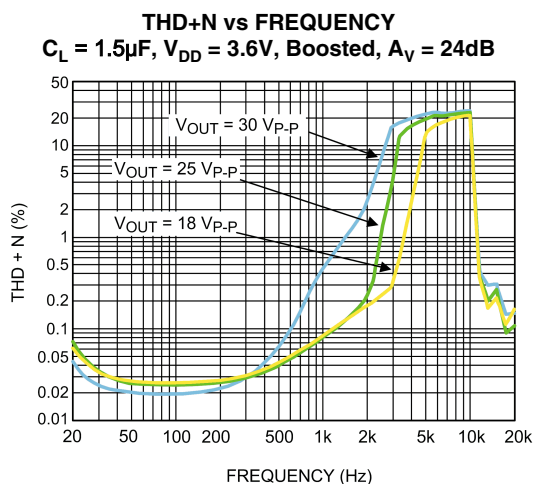
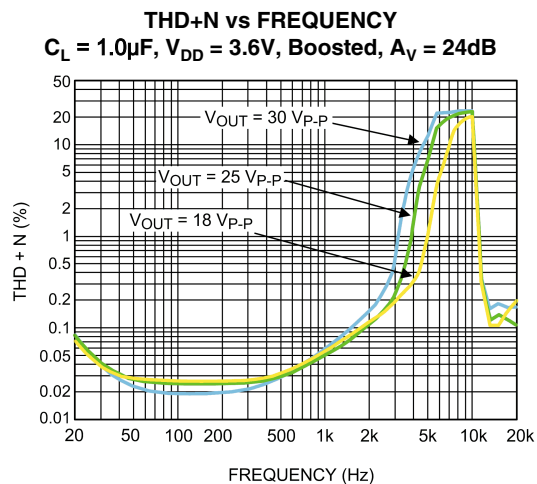
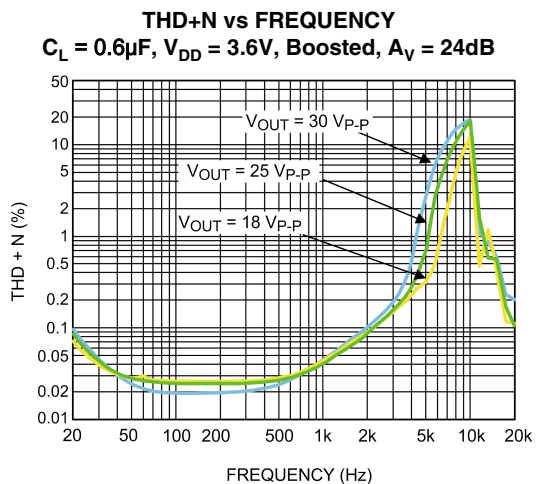


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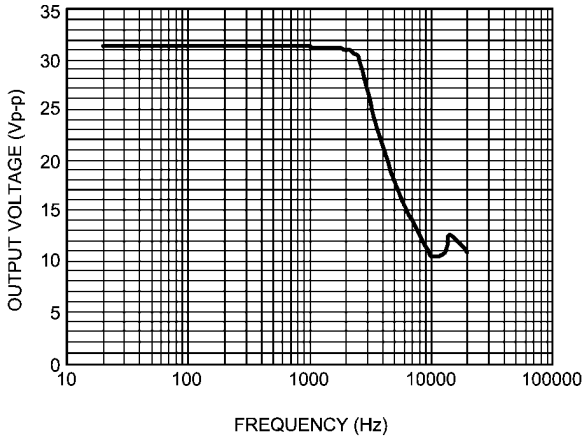
FIGURE 3. CMRR Test Circuit

## Typical Performance Characteristics

All typical performance curves are taken with conditions seen in [Figure 1](#) (Typical Application Circuit), unless otherwise specified.

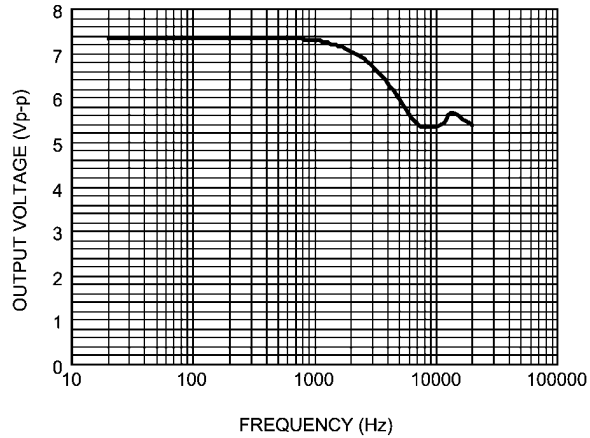


**OUTPUT VOLTAGE vs FREQUENCY**  
 $C_L = 1.5\mu\text{F}$ , THD+N  $\leq 1\%$ , Boosted



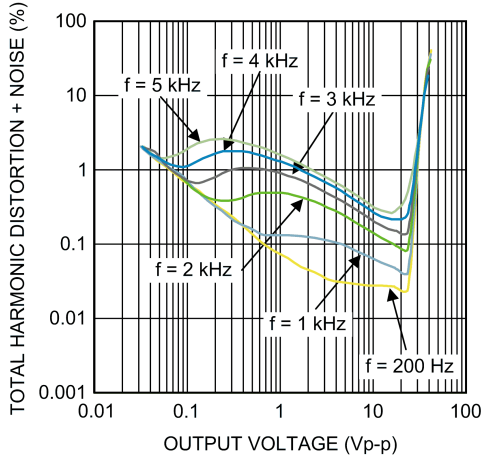
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**OUTPUT VOLTAGE vs FREQUENCY**  
 $C_L = 1.5\mu\text{F}$ , THD+N  $\leq 1\%$ , Unboosted



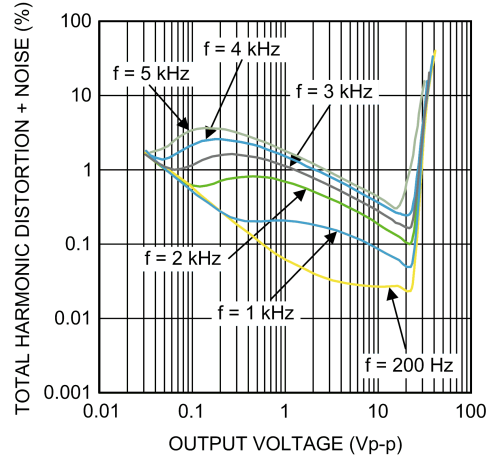
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**THD+N vs OUTPUT VOLTAGE**  
 $C_L = 0.6\mu\text{F}$ ,  $V_{DD} = 3.6\text{V}$ , Boosted,  $A_V = 24\text{dB}$



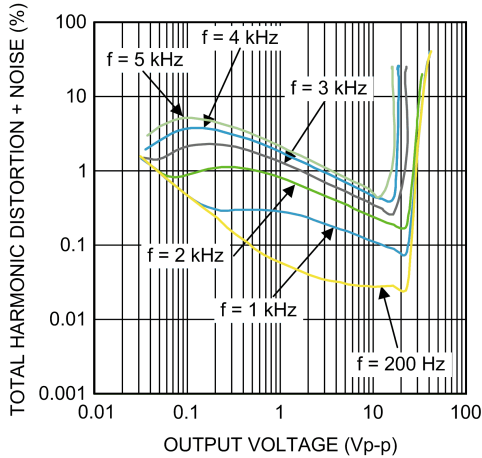
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**THD+N vs OUTPUT VOLTAGE**  
 $C_L = 1.0\mu\text{F}$ ,  $V_{DD} = 3.6\text{V}$ , Boosted,  $A_V = 24\text{dB}$



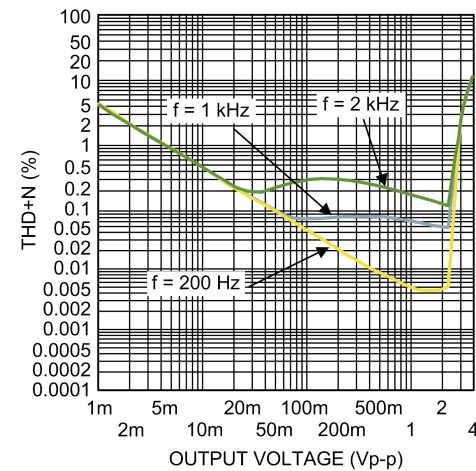
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**THD+N vs OUTPUT VOLTAGE**  
 $C_L = 1.5\mu\text{F}$ ,  $V_{DD} = 3.6\text{V}$ , Boosted,  $A_V = 24\text{dB}$



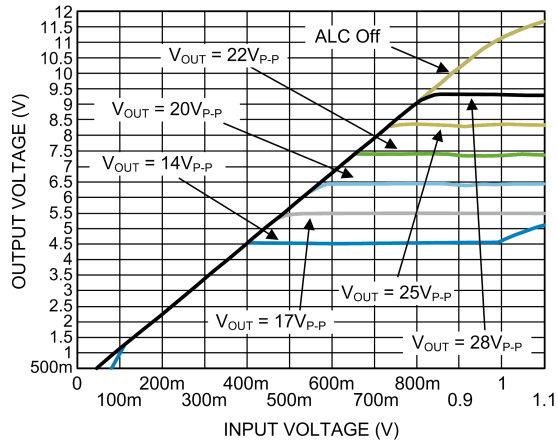
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**THD+N vs OUTPUT VOLTAGE**  
 $C_L = 1.5\mu\text{F}$ ,  $V_{DD} = 3.6\text{V}$ , Unboosted,  $A_V = 0\text{dB}$



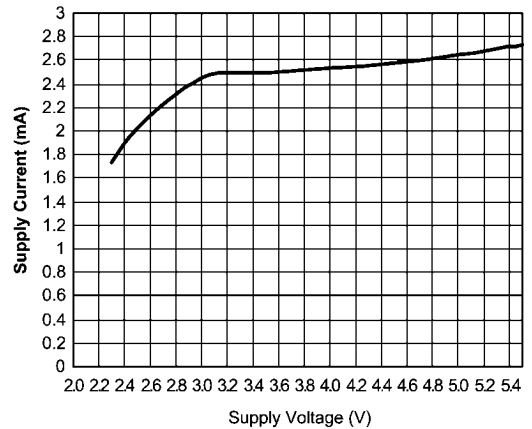
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**INPUT VOLTAGE vs OUTPUT VOLTAGE**  
ALC Enabled,  $A_V = 21\text{dB}$ ,  $V_{DD} = 3.6\text{V}$



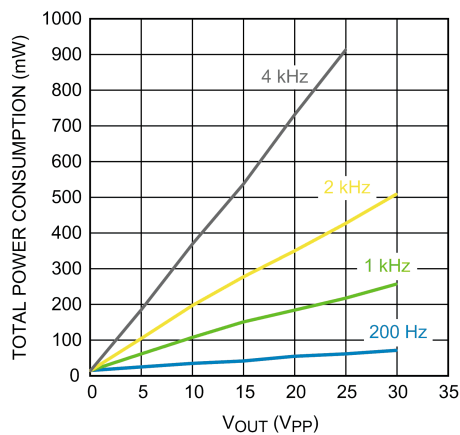
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**SUPPLY CURRENT vs SUPPLY VOLTAGE**  
 $R_L = \infty$



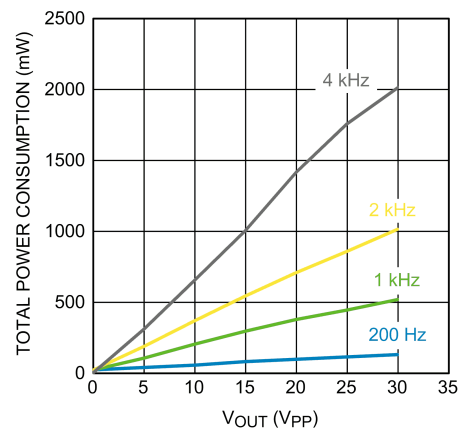
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**TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE**  
 $V_{DD} = 3.6\text{V}$ ,  $C_L = 0.6\mu\text{F}$



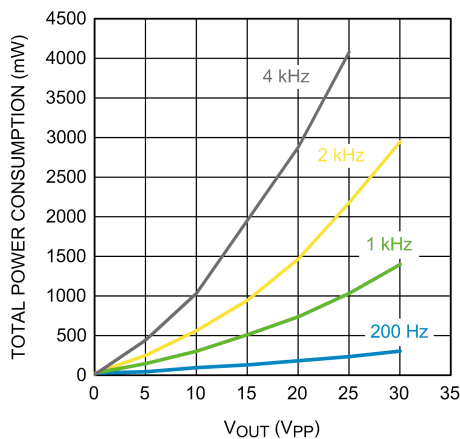
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**TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE**  
 $V_{DD} = 3.6\text{V}$ ,  $C_L = 1.0\mu\text{F}$



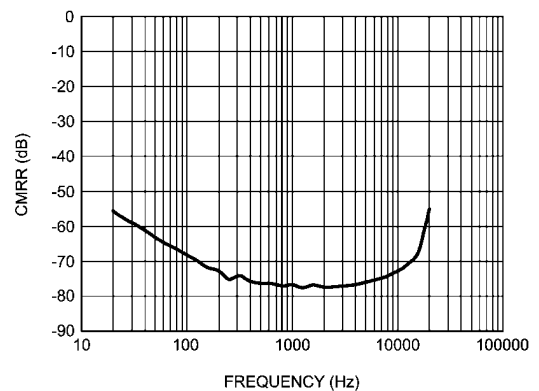
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**TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE**  
 $V_{DD} = 3.6\text{V}$ ,  $C_L = 1.5\mu\text{F}$



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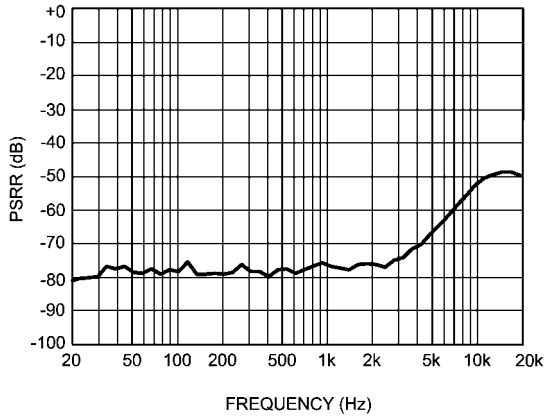
**COMMON MODE REJECTION RATIO vs FREQUENCY**  
 $V_{CM} = 200\text{mV}_{P-P}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $V_{DD} = 3.6\text{V}$ ,  $C_L = 1.5\mu\text{F}$



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**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

$V_{\text{RIPPLE}} = 200\text{mV}_{\text{p-p}}$ ,  $V_{\text{DD}} = 3.6\text{V}$ ,  $C_{\text{L}} = 1.5\mu\text{F}$



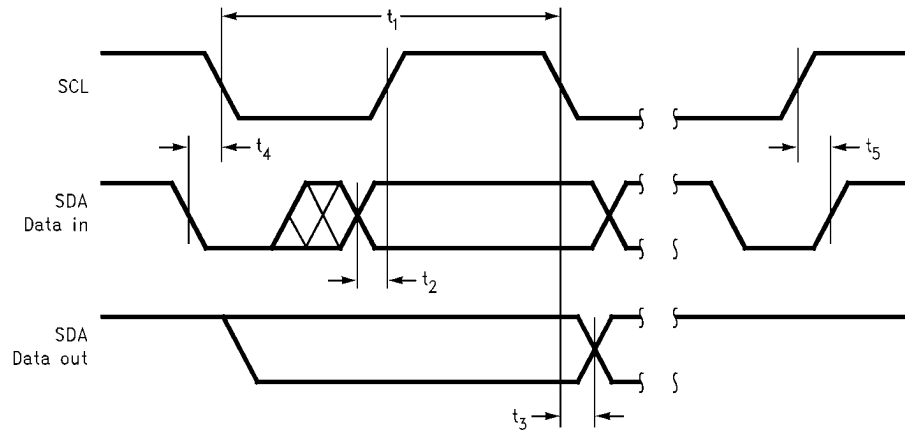
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## Application Information

### READ/WRITE I<sup>2</sup>C COMPATIBLE INTERFACE

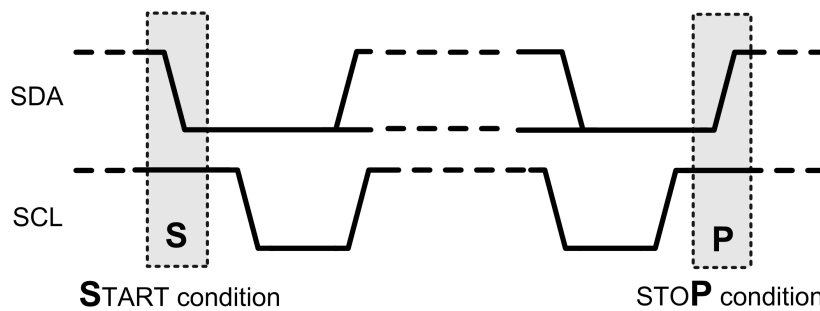
The LM48560 is controlled through an I<sup>2</sup>C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48560 and the master can communicate at clock rates up to 400kHz. [Figure 4](#) shows the I<sup>2</sup>C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48560 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition [Figure 5](#). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse [Figure 6](#). The LM48560 device address is 1101111.

### I<sup>2</sup>C BUS FORMAT



30150740

FIGURE 4. I<sup>2</sup>C Timing Diagram



30150741

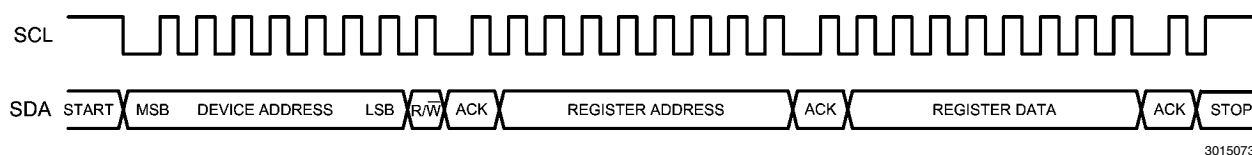
FIGURE 5. Start and Stop Diagram

### WRITE SEQUENCE

The example write sequence is shown in *Figure 6*. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the  $R/\overline{W}$  bit ( $R/\overline{W} = 0$  indicating the master is writing to the LM48560). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the  $R/\overline{W}$  bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48560 sends another ACK bit. Upon receipt of the acknowledge, the 8-bit register data is sent, MSB first. The register data word is followed by an ACK, upon receipt of which, the master issues a STOP bit, allowing SDA to go high while SDA is high.

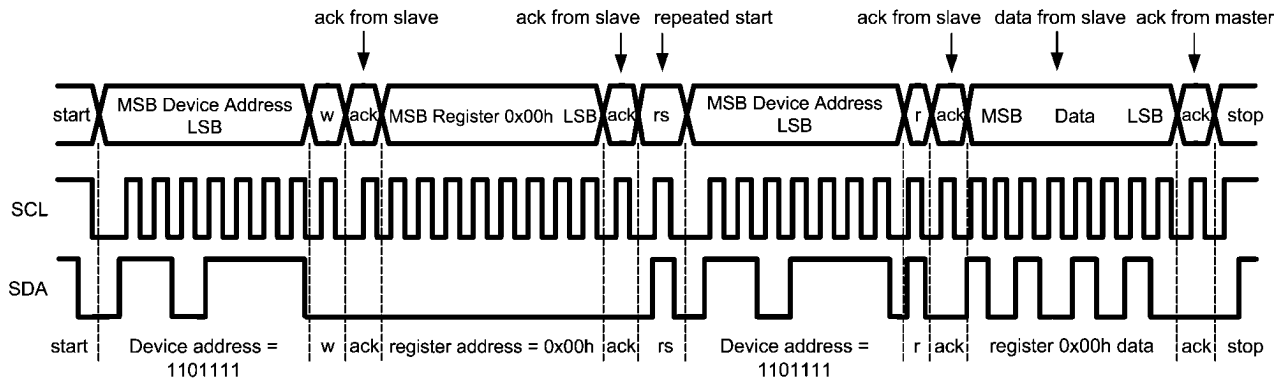


**FIGURE 6. Example I<sup>2</sup>C Write Cycle**

### READ SEQUENCE

The example read sequence is shown in *Figure 7*. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, followed by the  $R/\overline{W} = 1$  ( $R/\overline{W} = 1$  indicating the master wants to read data from the LM48560). After the  $R/\overline{W}$  bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK). Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first, followed by an ACK and selected register data from the LM48560. The register data is sent MSB first. Following the acknowledgement of the register data word [7:0], the master issues a STOP bit, allowing SDA to go high while SDA is high.



**FIGURE 7. Example I<sup>2</sup>C Read Cycle**

**TABLE 2. Device Address**

|                | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 (R/W) |
|----------------|----|----|----|----|----|----|----|----------|
| Device Address | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 0        |

**TABLE 3. Mode Selection**

| SW/HW | SDA/SEL               | SCL/GAIN | MODE                  |
|-------|-----------------------|----------|-----------------------|
| 0     | 0<br>(Boost Disabled) | 0        | IN1, $A_V = 0$        |
|       |                       | 1        | IN1, $A_V = 6$        |
|       | 1<br>(Boost Enabled)  | 0        | IN2, $A_V = 24$       |
|       |                       | 1        | IN2, $A_V = 30$       |
| 1     | X                     | X        | I <sup>2</sup> C Mode |

**TABLE 4. I<sup>2</sup>C Control Registers**

| REGISTER ADDRESS | Register Name    | B7 | B6   | B5   | B4   | B3      | B2     | B1       | B0    |
|------------------|------------------|----|------|------|------|---------|--------|----------|-------|
| 0x00h            | SHUTDOWN CONTROL | X  | X    | X    | X    | TURN_ON | IN_SEL | BOOST_EN | SHDN  |
| 0x01h            | NO CLIP CONTROL  | X  | RLT1 | RLT0 | ATK1 | ATK0    | PLEV2  | PLEV1    | PLEV0 |
| 0x02h            | GAIN CONTROL     | X  | X    | X    | X    | X       | X      | GAIN1    | GAIN0 |
| 0x03h            | TEST MODE        | X  | X    | X    | X    | X       | X      | X        | X     |

**TABLE 5. Shutdown Control Register**

| BIT   | NAME     | VALUE | DESCRIPTION                                 |
|-------|----------|-------|---|
| B7:B4 | UNUSED   | X     | Unused, set to 0                            |
| B3    | TURN_ON  | 0     | Normal turn on time, $t_{WU} = 15\text{ms}$ |
|       |          | 1     | Fast turn on time, $t_{WU} = 5\text{ms}$    |
| B2    | IN_SEL   | 0     | Input 1 selected                            |
|       |          | 1     | Input 2 selected                            |
| B1    | BOOST_EN | 0     | Boost disabled                              |
|       |          | 1     | Boost enabled                               |
| B0    | SHDN     | 0     | Device shutdown                             |
|       |          | 1     | Device enabled                              |

**TABLE 6. No Clip Control Register**

| BIT   | NAME                                   | VALUE |    |    | DESCRIPTION   |
|-------|--|-------|----|----|---|
| B7    | UNUSED                                 | X     |    |    | Unused, set to 0  |
| B6:B5 | RLT1 (B6)<br>RLT0 (B5)                 | B6    | B5 |    | Sets Release Time based on $C_{SET}$ .<br>See "Release Time" section. |
|       |  | 0     | 0  |    | $T_R = 0.5s$  |
|       |  | 0     | 1  |    | $T_R = 0.38s$   |
|       |  | 1     | 0  |    | $T_R = 0.21s$   |
|       |  | 1     | 1  |    | $T_R = 0.17s$   |
| B4:B3 | ATK1 (B4)<br>ATK0 (B3)                 | B4    | B3 |    | Sets Attack Time based on $C_{SET}$ .<br>See "Attack Time" section.   |
|       |  | 0     | 0  |    | $T_A = 0.83ms$  |
|       |  | 0     | 1  |    | $T_A = 1.2ms$   |
|       |  | 1     | 0  |    | $T_A = 1.5ms$   |
|       |  | 1     | 1  |    | $T_A = 2.2ms$   |
| B2:B0 | PLEV2 (B2)<br>PLEV1 (B1)<br>PLEV0 (B0) | B2    | B1 | B0 | Sets output voltage limit level.                                      |
|       |  | 0     | 0  | 0  | Voltage Limit disabled  |
|       |  | 0     | 0  | 1  | $V_{TH(VLIM)} = 14V_{P-P}$  |
|       |  | 0     | 1  | 0  | $V_{TH(VLIM)} = 17V_{P-P}$  |
|       |  | 0     | 1  | 1  | $V_{TH(VLIM)} = 20V_{P-P}$  |
|       |  | 1     | 0  | 0  | $V_{TH(VLIM)} = 22V_{P-P}$  |
|       |  | 1     | 0  | 1  | $V_{TH(VLIM)} = 25V_{P-P}$  |
|       |  | 1     | 1  | 0  | $V_{TH(VLIM)} = 28V_{P-P}$  |
|       |  | 1     | 1  | 1  | Voltage Limit disabled  |

**TABLE 7. Gain Control Register**

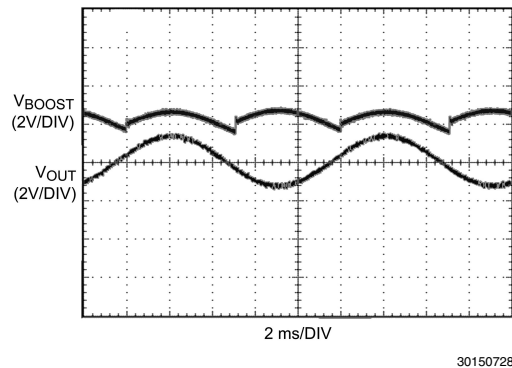
| BIT   | NAME                    | VALUE |    | DESCRIPTION   |
|-------|-------------------------|-------|----|---|
| B7:B2 | UNUSED                  | X     |    | Unused, set to 0                                      |
| B1:B0 | GAIN1(B1)<br>GAIN0 (B0) | B1    | B0 | Sets amplifier gain.<br>Boost disabled (BOOST_EN = 0) |
|       |                         | 0     | 0  | 0dB   |
|       |                         | 0     | 1  | 6dB   |
|       |                         | 1     | 0  | 12dB  |
|       |                         | 1     | 1  | 18dB  |
| B1:B0 | GAIN1(B1)<br>GAIN0 (B0) | B1    | B0 | Sets amplifier gain.<br>Boost enabled (BOOST_EN = 1)  |
|       |                         | 0     | 0  | 21dB  |
|       |                         | 0     | 1  | 24dB  |
|       |                         | 1     | 0  | 27dB  |
|       |                         | 1     | 1  | 30dB  |

### GENERAL AMPLIFIER FUNCTION

The LM48560 is a fully differential, Class H piezo driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier’s supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

### CLASS H OPERATION

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below  $3V_{P-P}$ , the nominal boost voltage is 6V. As the amplifier output increases above  $3V_{P-P}$ , the boost voltage tracks the amplifier output as shown in *Figure 8*. When the amplifier output falls below  $3V_{P-P}$ , the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.



**FIGURE 8. Class H Operation**

### DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48560 features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

### AUTOMATIC LEVEL CONTROL (ALC)

The ALC is available in software mode only, and only in boosted mode. In hardware mode ALC is always disabled. The ALC limits the peak output voltage to the programmed value. Consequently, it limits the peak boost voltage, as this is derived from the output voltage. The ALC is continuous, in that it provides a continuous adjustment of the voltage gain in order to limit the output voltage to the programmed value. The available gain adjustment range is typically 8dB. When the input amplitude is further increased beyond the ALC attenuation range, the output will again increase. This is illustrated in the Typical Performance Graphs, as seen on the  $14V_{PP}$  plot in the Input voltage vs Output Voltage curve. The attack and decay of the ALC is programmed by software and works in conjunction with the external capacitor  $C_{SET}$ . Typically  $C_{SET}$  is  $0.1\mu F$ , although it can be changed from  $0.1\mu F$  to  $4.7\mu F$  to select other ranges of attack and decay time.

### ATTACK TIME

Attack time ( $t_{ATK}$ ) is the time it takes for the gain to be reduced by 6dB once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of  $C_{SET}$  and the attack time coefficient as given by equation (2):

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (1)$$

Where  $\alpha_{ATK}$  is the attack time coefficient ( ) set by bits B4:B3 in the Voltage Limit Control Register (see ). The attack time coefficient allows the user to set a nominal attack time. The internal  $20k\Omega$  resistor is subject to temperature change, and it has tolerance between -11% to +20%.

**TABLE 8. Attack Time Coefficient**

| B4 | B3 | $\alpha_{ATK}$ |
|----|----|----------------|
| 0  | 0  | 2.4            |
| 0  | 1  | 1.7            |
| 1  | 0  | 1.3            |
| 1  | 1  | 0.9            |

**RELEASE TIME**

Release time ( $t_{RL}$ ) is the time it takes for the gain to return from 6dB to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of  $C_{SET}$  and release time coefficient as given by equation (3):

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \quad (2)$$

where  $\alpha_{RL}$  is the release time coefficient (Table 9) set by bits B6:B5 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20M $\Omega$  is subject to temperature change, and it has tolerance between -11% to +20%.

**TABLE 9. Release Time Coefficient**

| B6 | B5 | $\alpha_{RL}$ |
|----|----|---------------|
| 0  | 0  | 4             |
| 0  | 1  | 5.3           |
| 1  | 0  | 9.5           |
| 1  | 1  | 11.8          |

**BOOST CONVERTER**

The LM48560 features an integrated boost converter with a dynamic output control. The device monitors the output signal of the amplifier, and adjusts the output voltage of the boost converter to maintain sufficient headroom while improving efficiency.

**SOFTWARE/HARDWARE MODE**

Device operation in hardware or software mode is determined by the state of the SW/ $\overline{HW}$  pin. Connect SW/ $\overline{HW}$  to ground for hardware mode, and connect to  $V_{DD}$  for software mode.

| SW/ $\overline{HW}$ | SDA/SEL               | SCL/GAIN | MODE                  |
|---------------------|-----------------------|----------|-----------------------|
| 0                   | 0<br>(Boost Disabled) | 0        | IN1, $A_v = 0$        |
|                     |                       | 1        | IN1, $A_v = 6$        |
|                     | 1<br>(Boost Enabled)  | 0        | IN2, $A_v = 24$       |
|                     |                       | 1        | IN2, $A_v = 30$       |
| 1                   | SDA                   | SCL      | I <sup>2</sup> C Mode |

**GAIN SETTING**

The LM48560 features four internally configured gain settings 0db, 6dB, and 30dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in [Table 10](#).

**TABLE 10. Gain Setting**

| GAIN | GAIN SETTING<br>IN1 | GAIN SETTING<br>IN2 |
|------|---------------------|---------------------|
| 0    | 0dB                 | 24dB                |
| 1    | 6dB                 | 30dB                |

## SHUTDOWN FUNCTION

The LM48560 features a low current shutdown mode. Set  $\overline{SD} = \text{GND}$  to disable the amplifier and boost converter and reduce supply current to 0.01  $\mu\text{A}$ .

## SINGLE-ENDED INPUT CONFIGURATION

The LM48560 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. [Figure 9](#) shows the typical single-ended applications circuit.

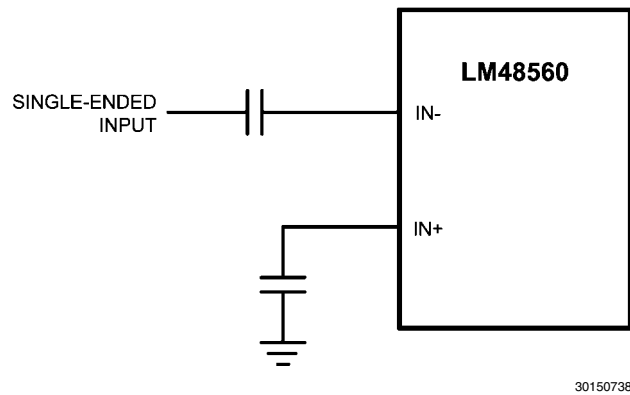


FIGURE 9. Single-Ended Input Configuration

## PROPER SELECTION OF EXTERNAL COMPONENTS

### ALC Timing ( $C_{\text{SET}}$ ) Capacitor Selection

The recommended range value of  $C_{\text{SET}}$  is between .01  $\mu\text{F}$  to 1  $\mu\text{F}$ . Lowering the value below .01  $\mu\text{F}$  can increase the attack time but LM48560 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD +N and audio quality will be severely affected.

### Power Selection of External Components

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1  $\mu\text{F}$  ceramic capacitor from  $V_{\text{DD}}$  to GND. Additional bulk capacitance may be added as required.

### Boost Converter Capacitor Selection

The LM48560 boost converter requires three external capacitors for proper operation: a 1  $\mu\text{F}$  supply bypass capacitor, and 1  $\mu\text{F}$  + 100 pF output reservoir capacitors. Place the supply bypass capacitor as close to  $V_{\text{DD}}$  as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended. See Table 4 for suggested capacitor manufacturers.

### Inductor Selection

The LM48560 boost converter is designed for use with a 4.7  $\mu\text{H}$  inductor. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48560 (> 1A). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

### Diode Selection

Use a Schottkey diode as shown in [Figure 1](#). A 20V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500mA.

## PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48560 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

## DEMO BOARD USER GUIDE

### Quick Start Guide (Hardware Mode):

1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 2 and 3(GND) of JU7 to set the device in hardware mode.
3. Short pins 2 and 3 (GND) of JU3 to select IN1.
4. Short pins 2 and 3 (GND) of JU2 for 0dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Power on the board and observe the output on OUT+ and OUT-

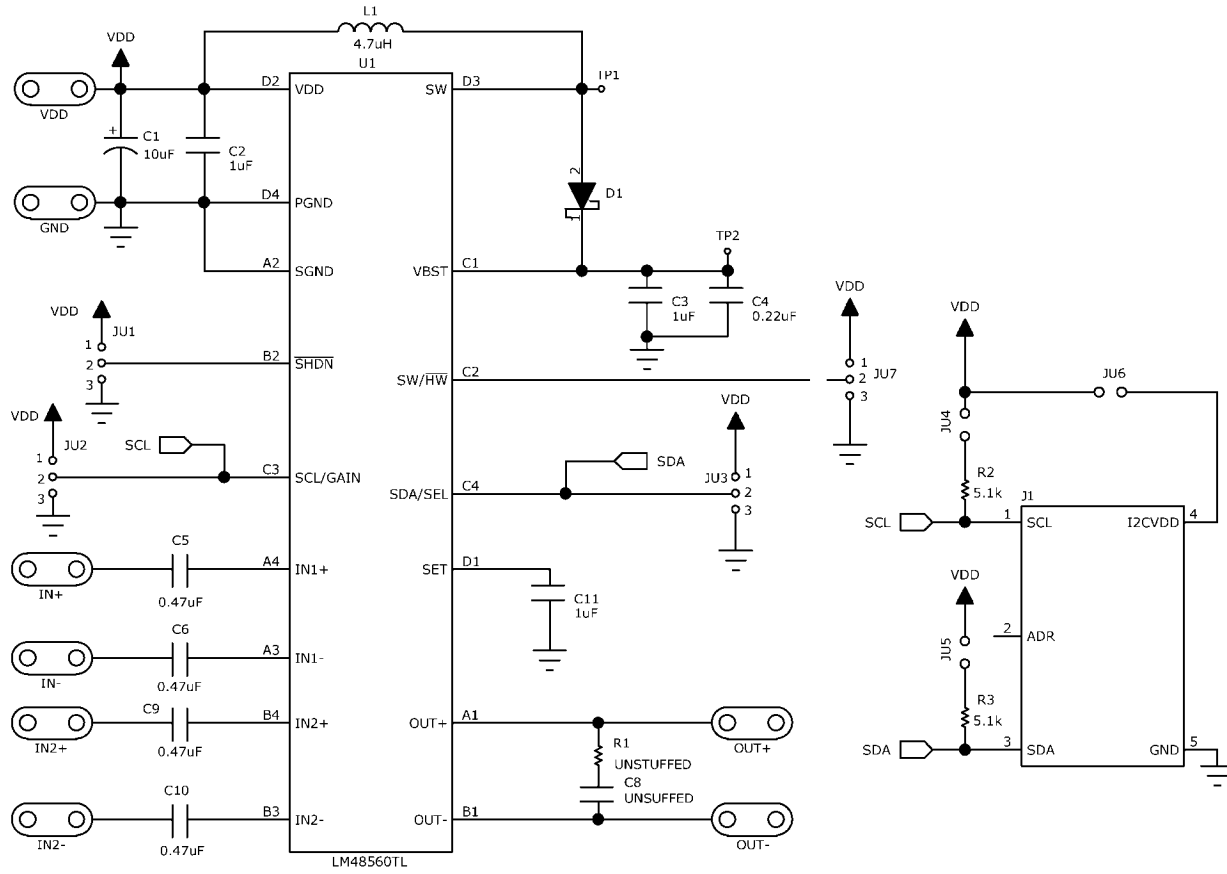
### Quick Start Guide (Software Mode):

1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 1 (VDD) and 2 of JU7 to set the device in software mode.
3. Short pins 1 (VDD) and 2 of JU3 to select IN2.
4. Short pins 2 and 3 (GND) of JU2 for 24dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Connect the USB/I2C board to the LM48560 demo board.
8. Connect the USB/I2C board to a PC
9. Turn on the power supply
10. Launch the LM48560 software GUI
11. Verify that the bottom left corner of the GUI reads "USB Connected ALL ACK" (note 1)
12. Select the following:
  - a. INPUT SELECT = INPUT 1
  - b. BOOST = ON
  - c. TURN ON TIME = NORMAL
  - d. GAIN = 0dB

**Note:** If the GUI reads "USB I/O error NAK" the device has not been acknowledged, please double check your connections.

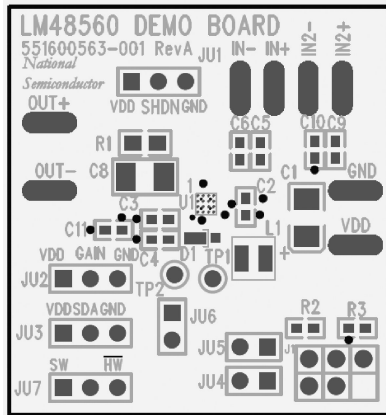
| Header Functionality |                  |  |
|----------------------|------------------|--|
| Designator           | Function         | Notes  |
| VDD                  | VDD              | Power Supply   |
| GND                  | GND              | Ground reference   |
| OUT+                 | OUTPUT           | Positive output terminal   |
| OUT-                 | OUTPUT           | Negative output terminal   |
| IN1+                 | INPUT 1          | Positive input terminal 1  |
| IN1-                 | INPUT 1          | Negative input terminal 1  |
| IN2+                 | INPUT 2          | Positive input terminal 2  |
| IN2-                 | INPUT 2          | Negative input terminal 2  |
| JU1                  | Shutdown         | Short pin 1 (VDD) and pin 2 for normal operation Short pin 2 and pin 3 (GND) for device shutdown   |
| JU2                  | SCL/Gain Select  | Hardware mode: Short pin 2 to pin 1 (VDD) for higher gain. Short pin 2 to pin 3(GND) for lower gain. (See Table 10) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication |
| JU3                  | SDA/Input Select | Hardware mode: Short pin 2 to pin 1 (VDD) to select IN2. Short pin 2 to pin 3 (GND) to select IN1. (See Table 10) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication   |
| JU4                  | SCL Pullup       | Short JU4 to connect pullup resistor to VDD. Open to use external I2C supply voltage   |
| JU5                  | SDA pullup       | Short JU5 to connect pullup resistor to VDD. Open to use external I2C supply voltage   |
| JU6                  | I2C VDD          | Short JU6 to use VDD as I2C VDD. Open to use external I2C supply voltage   |
| JU7                  | SW/HW            | Software Mode: Short pins 1 (VDD) and 2 Hardware Mode: Short pins 2 and 3(GND)   |

Demo Board Schematic



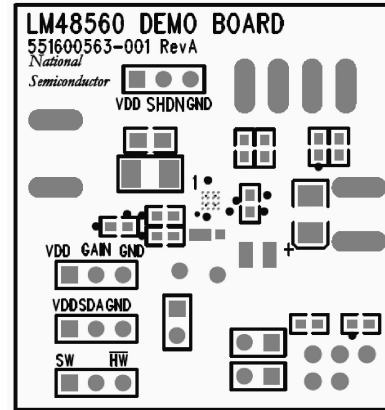
30150779

## PC Board Layout



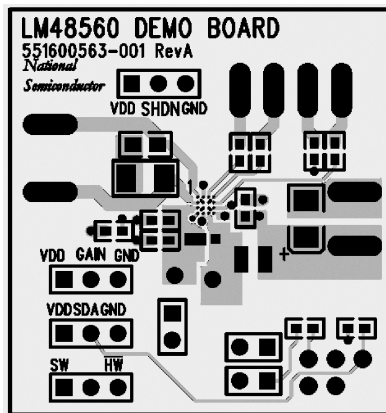
Top Silk Screen

30150769



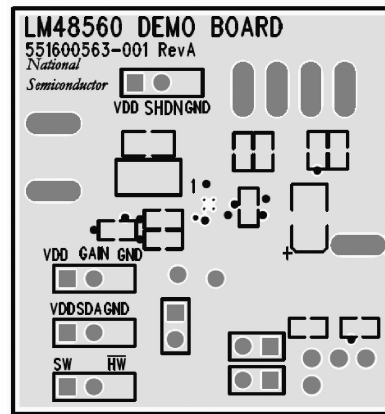
Solder Mask Top

30150771



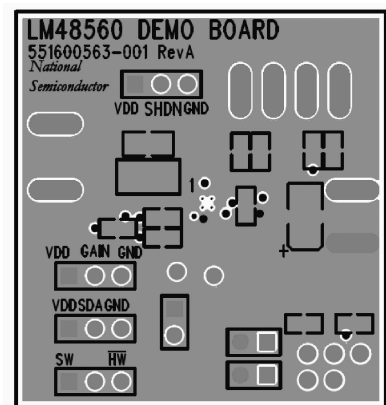
Top Layer

30150772



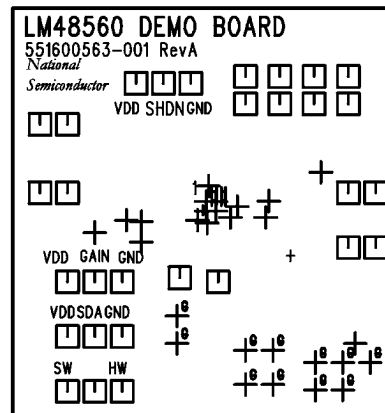
Layer 2

30150766



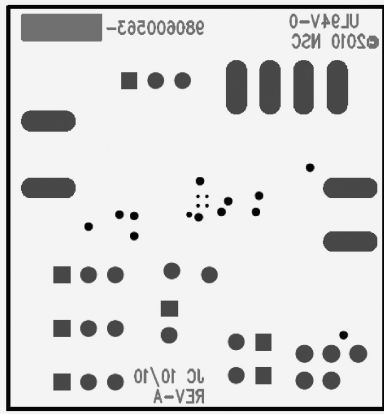
Layer 3

30150765



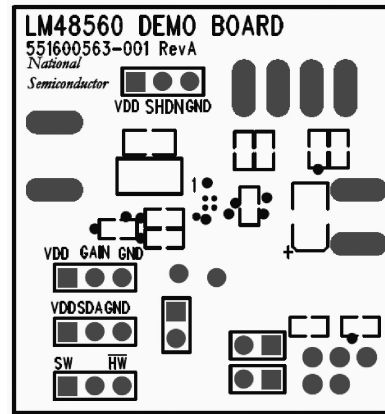
Drill Drawing

30150764



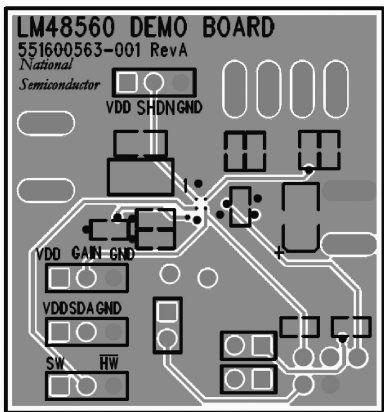
Silk Bottom

30150768



Solder Mask Bottom

30150770



Bottom Layer

30150763

## Revision History

| <b>Rev</b> | <b>Date</b> | <b>Description</b>  |
|------------|-------------|---|
| 1.0        | 08/16/11    | Initial WEB released.   |
| 1.01       | 09/21/11    | Input edits under CLASS H OPERATION.  |
| 1.02       | 11/01/11    | Edited curves 30150753, 54, 55, 56, and Figure 7 (I <sup>2</sup> C Read Cycle). |
| 1.03       | 11/10/11    | Edited Figure 7.  |
| 1.04       | 07/25/12    | Input texts/limits edits in the EC table.                                       |
| 1.05       | 08/22/12    | Edited Tables 8 and 9.  |



# Notes

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| RFID                   | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
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